

Power MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	100
R _{DS(on)} (Ω)	V _{GS} = 10 V 0.54
Q _g max. (nC)	8.3
Q _{gs} (nC)	2.3
Q _{gd} (nC)	3.8
Configuration	Single

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- 175 °C operating temperature
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



Available
RoHS*
Available

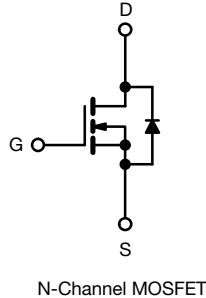
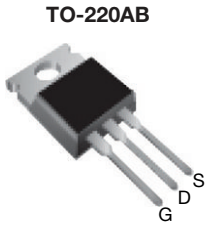
Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.



N-Channel MOSFET

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF510PbF
	SiHF510-E3
SnPb	IRF510
	SiHF510

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL		LIMIT	UNIT	
Drain-Source Voltage	V _{DS}		100	V	
Gate-Source Voltage	V _{GS}		± 20		
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	5.6	A	
		T _C = 100 °C	4.0		
Pulsed Drain Current ^a	I _{DM}		20		
Linear Derating Factor			0.29	W/°C	
Single Pulse Avalanche Energy ^b	E _{AS}		75	mJ	
Repetitive Avalanche Current ^a	I _{AR}		5.6	A	
Repetitive Avalanche Energy ^a	E _{AR}		4.3	mJ	
Maximum Power Dissipation	T _C = 25 °C		P _D	43	W
Peak Diode Recovery dV/dt ^c	dV/dt		5.5	V/ns	
Operating Junction and Storage Temperature Range	T _J , T _{stg}		-55 to +175	°C	
Soldering Recommendations (Peak temperature) ^d	for 10 s		300		
Mounting Torque	6-32 or M3 screw		10	lbf · in	
			1.1	N · m	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = 25 V, starting T_J = 25 °C, L = 4.8 mH, R_g = 25 Ω, I_{AS} = 5.6 A (see fig. 12).
- I_{SD} ≤ 5.6 A, dI/dt ≤ 75 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C.
- 1.6 mm from case.



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.5	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	0.12	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 3.4\text{ A}^b$	-	-	0.54	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 3.4\text{ A}^b$	1.3	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz},$ see fig. 5	-	180	-	pF
Output Capacitance	C_{oss}		-	81	-	
Reverse Transfer Capacitance	C_{rss}		-	15	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$ $I_D = 5.6\text{ A}, V_{DS} = 80\text{ V}$ $V_{DS} = 10\text{ V},$ see fig. 6 and fig. 13 ^b	-	-	8.3	nC
Gate-Source Charge	Q_{gs}		-	-	2.3	
Gate-Drain Charge	Q_{gd}		-	-	3.8	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, I_D = 5.6\text{ A}$ $R_g = 24\text{ }\Omega, R_D = 8.4\text{ }\Omega,$ see fig. 10 ^b	-	6.9	-	ns
Rise Time	t_r		-	16	-	
Turn-Off Delay Time	$t_{d(off)}$		-	15	-	
Fall Time	t_f		-	9.4	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	5.6	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	20	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 5.6\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	2.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 5.6\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	100	200	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.44	0.88	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\text{ }\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

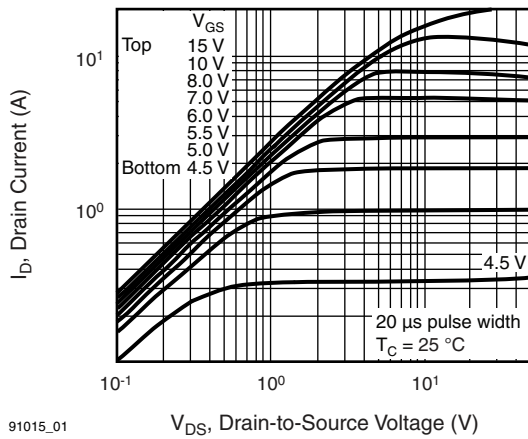


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

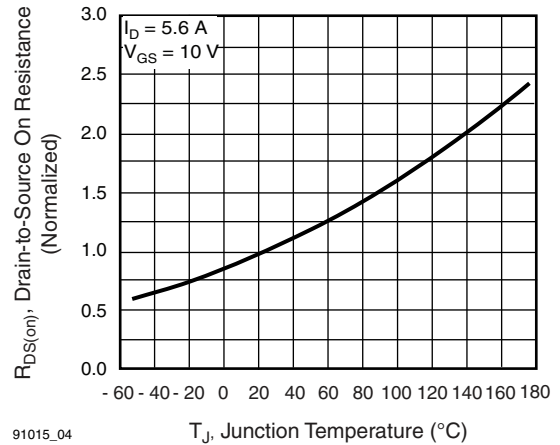


Fig. 4 - Normalized On-Resistance vs. Temperature

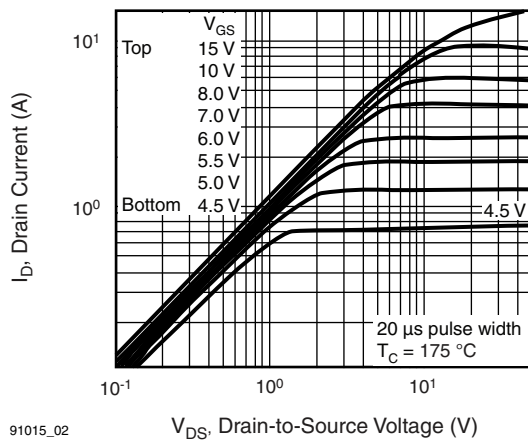


Fig. 2 - Typical Output Characteristics, $T_C = 175\text{ }^\circ\text{C}$

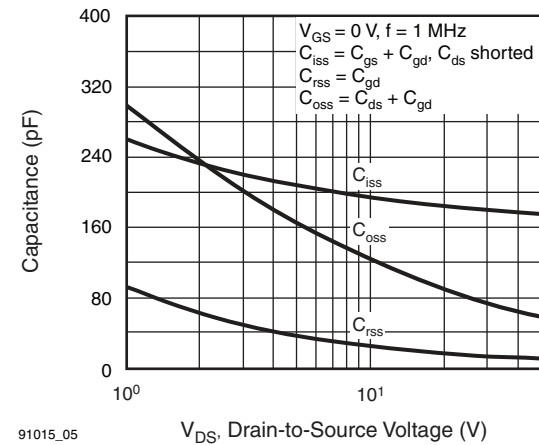


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

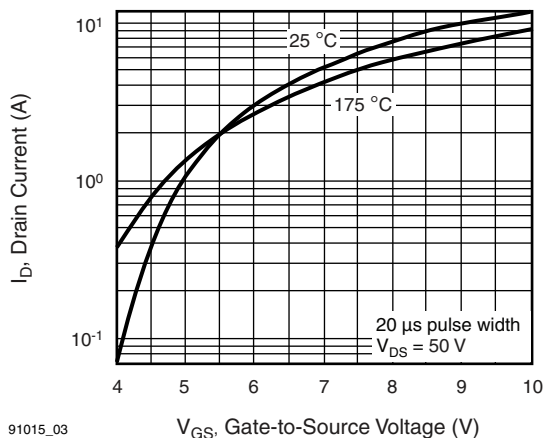


Fig. 3 - Typical Transfer Characteristics

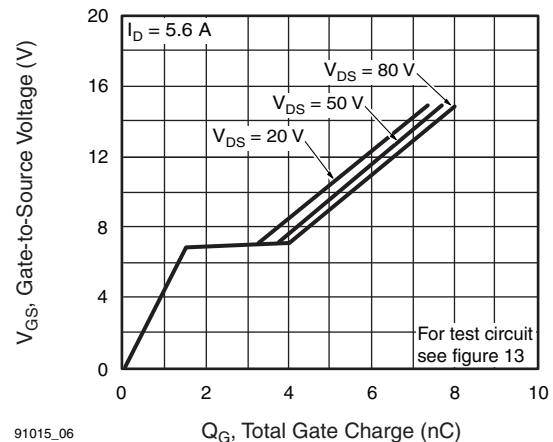


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 9 - Maximum Drain Current vs. Case Temperature



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Fig. 8 - Maximum Safe Operating Area

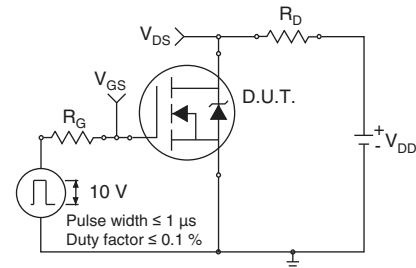


Fig. 10a - Switching Time Test Circuit

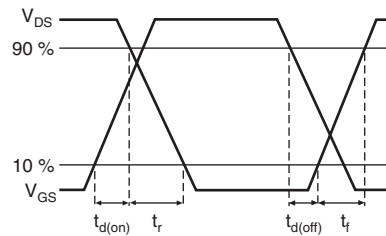


Fig. 10b - Switching Time Waveforms



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Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



Fig. 12a - Unclamped Inductive Test Circuit



Fig. 13a - Basic Gate Charge Waveform

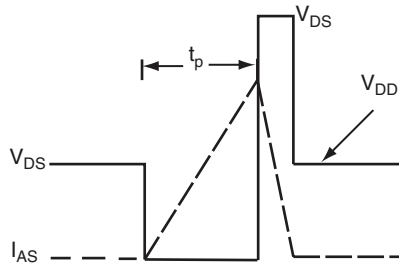


Fig. 12b - Unclamped Inductive Waveforms

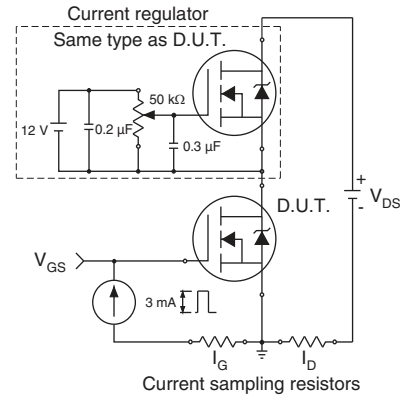


Fig. 13b - Gate Charge Test Circuit

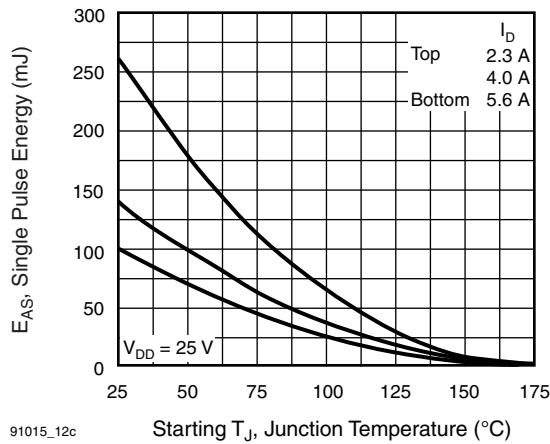
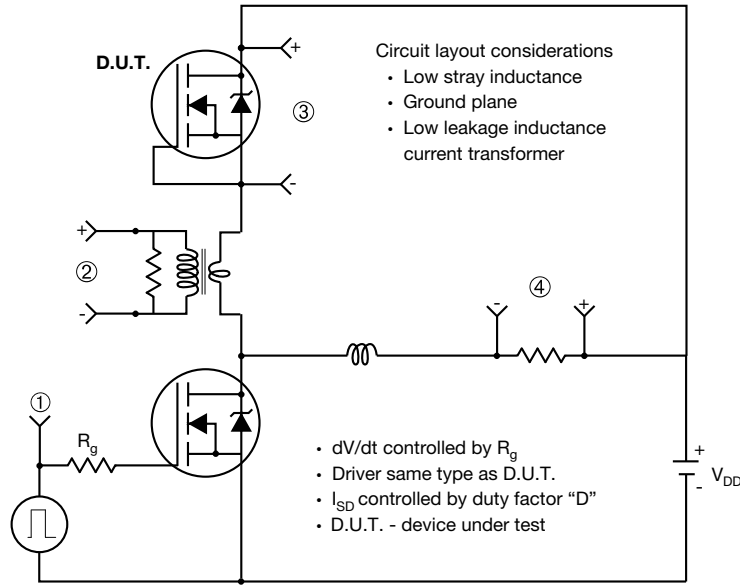


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Peak Diode Recovery dV/dt Test Circuit



Note
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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